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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/576,570	04/19/2006	Emmanuel Alie	FR03 0127 US1	3885
65913	7590	03/11/2008	EXAMINER	
NXP, B.V. NXP INTELLECTUAL PROPERTY DEPARTMENT M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			CHANG, DANIEL D	
			ART UNIT	PAPER NUMBER
			2819	
			NOTIFICATION DATE	DELIVERY MODE
			03/11/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No. 10/576,570	Applicant(s) ALIE, EMMANUEL	
	Examiner Daniel D. Chang	Art Unit 2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 April 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 and 5-7 is/are rejected.
- 7) ☒ Claim(s) 4 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 April 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>4/19/2006</u> . | 6) <input type="checkbox"/> Other: _____ |

Claim Objections

Claim 7 is objected to because of the following informalities: on line 1, the wording, “comprising comprising,” is redundant. It should be changed to “comprising:” Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-3 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takabayashi et al. (US 6,377,083 B1) in view of McGlinchey.

Regarding claim 1, Takabayashi discloses, in Figs. 3, 4, and 8, a method of powering an integrated circuit (10 in Figs. 3, 8), said integrated circuit comprising a chip (inherent for an IC) within a package assembly (inherent for an IC), said chip comprising a plurality of logic circuits (1), each of the logic circuits having at least one power input (2, 3), which should not receive a power voltage exceeding a predetermined operating voltage (col. 7, lines 37+), the method comprising the steps of:

measuring the power voltage (5 Vdd) supplied to the integrated circuit, and
regulating this power voltage in order to keep the difference between the measured voltage and a reference voltage (Vref) as small as possible (col. 7, lines 37+),

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wherein during the measuring step the power voltage is directly measured within the chip (see 7) at the power input of at least one of the logic circuits, and

wherein the method comprises the step of setting the reference voltage such that the voltage supplied to the power input of at least one logic circuit of the chip is equal to the predetermined operating voltage of this logic circuit (col. 7, lines 37+).

Takabayashi does not specifically disclose controlling the voltage supplied to the power input of logic circuit to be equal to or not exceeding a predetermined maximum operating voltage.

McGlinchey discloses, in Fig. 1, a window comparator circuit 2 that determines whether the voltage at input terminal is above, below or within a window voltage range.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have substituted the comparator 21 of Takabayashi with the window comparator 2 as taught by McGlinchey in order to controlling the voltage supplied to the power input of logic circuit to be equal to or not exceeding a predetermined maximum operating voltage.

Claims 5 and 7 are essentially the same in scope as claim 1 and is rejected similarly.

Regarding claims 2, 3, 6, and 7, as for the recitation, “known to be the first to be damaged” and “highest power voltage available within the chip” and “ it has been held that a recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Allowable Subject Matter

Claim 4 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barrie can be reached on (571) 272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Daniel D. Chang/

Primary Examiner, Art Unit 2819